

ME451: Control Systems

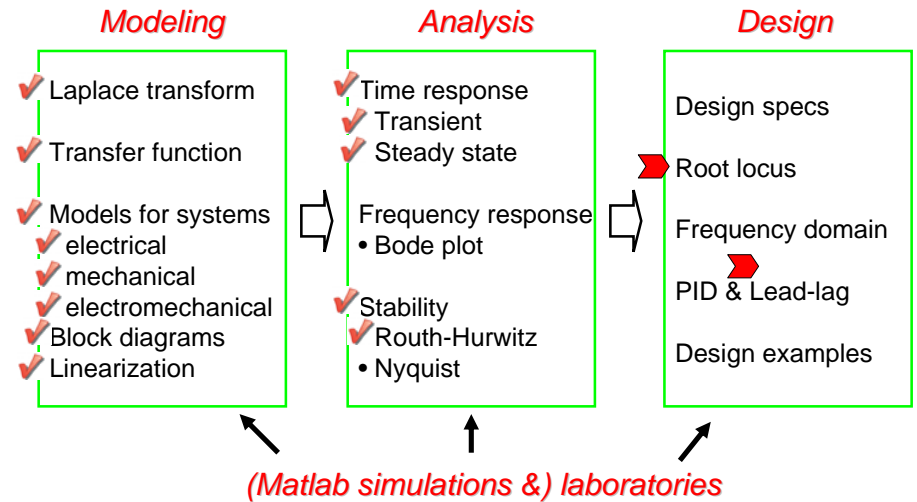
Lecture 21

Root locus: Lag compensator & Lead-lag compensator design

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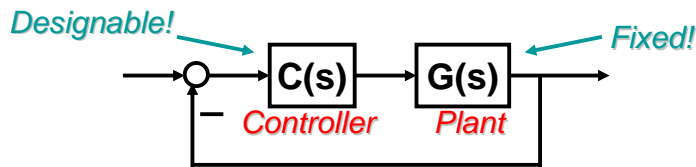
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Course roadmap



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Closed-loop design by root locus

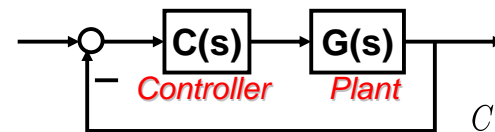


- Place closed-loop poles at desired location
 - by tuning the gain $C(s)=K$.
- If root locus does not pass the desired location, then reshape the root locus
 - by adding poles/zeros to $C(s)$.

Compensation

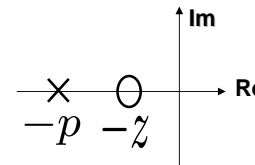
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Lead and lag compensators (review)

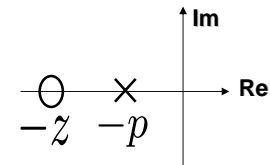


$$C(s) = K \frac{s+z}{s+p}, \quad (z > 0, p > 0)$$

- Lead compensator



- Lag compensator

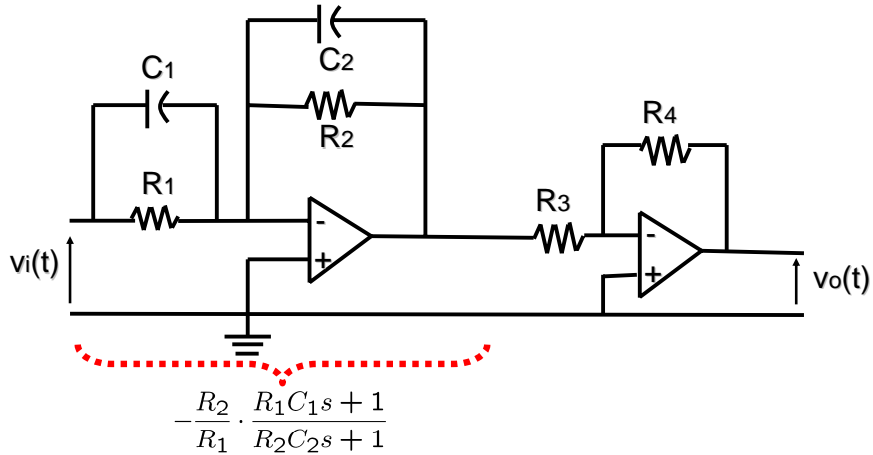


The reason why these are called “lead” and “lag” will be explained in frequency response approach (later in this course).

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Compensator realization

- One example, using operational amplifiers



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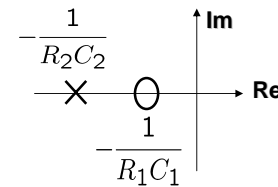
Compensator realization (cont'd)

- Transfer function

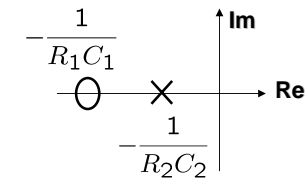
$$C(s) = \frac{V_o(s)}{V_i(s)} = \frac{R_2 R_1 C_1 (s + \frac{1}{R_1 C_1}) R_4}{R_1 R_2 C_2 (s + \frac{1}{R_2 C_2}) R_3} = \frac{R_4 C_1}{R_3 C_2} \frac{s + \frac{1}{R_1 C_1}}{s + \frac{1}{R_2 C_2}}$$

\uparrow K
 \uparrow z
 \downarrow p

- Lead compensator



- Lag compensator



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Roles of lead and lag compensators

- Lead compensator (Done)

- Improve transient response
- Improve stability

$$C_{Lead}(s) = K_1 \frac{s + z_1}{s + p_1}$$

- Lag compensator (Today)

- Reduce steady state error

$$C_{Lag}(s) = K_2 \frac{s + z_2}{s + p_2}$$

- Lead-lag compensator (Today)

- Take into account all the above issues.

$$C_{LL}(s) = C_{Lead}(s)C_{Lag}(s)$$

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Radar tracking system

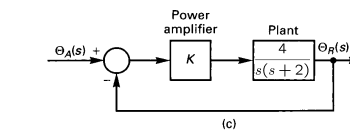
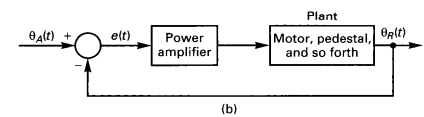
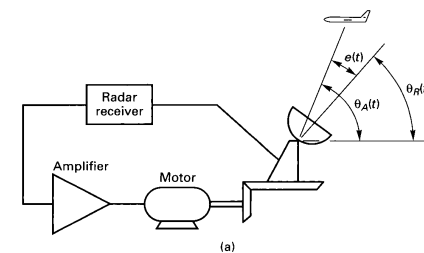


Figure 7.1 Radar tracking system.

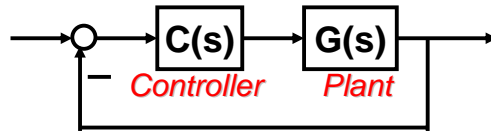


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Lead-lag compensator design

- Consider a system

$$G(s) = \frac{4}{s(s+2)}$$

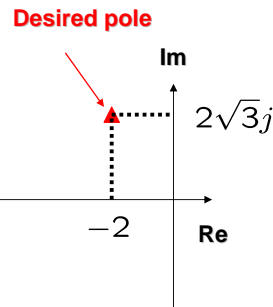


- Analysis of CL system for C(s)=1

- Damping ratio $\zeta=0.5$
- Undamped natural freq. $\omega_n=2$ rad/s
- Ramp-error constant $K_v=2$

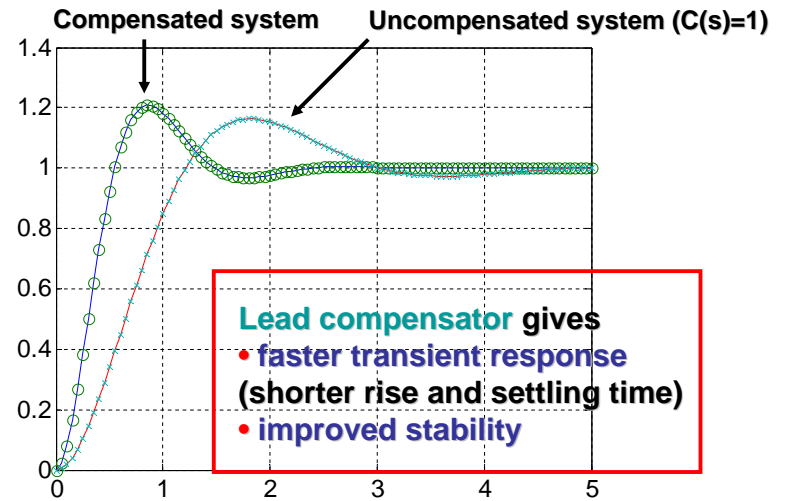
- Performance specification

- Damping ratio $\zeta=0.5$
- Undamped natural freq. $\omega_n=4$ rad/s
- Ramp-error constant $K_v=50$



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Comparison of step responses (after lead compensation)



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Error constants (after lead compensation)

$$G(s)C_{Lead}(s) = \frac{4}{s(s+2)} \cdot \frac{4.675(s+2.9)}{s+5.4}$$

- Step-error constant

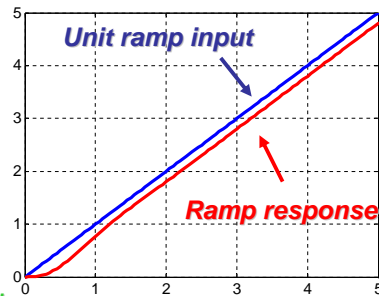
$$K_p := \lim_{s \rightarrow 0} G(s)C_{lead}(s) = \infty$$

- Ramp-error constant

$$K_v := \lim_{s \rightarrow 0} sG(s)C_{lead}(s) = 5.02$$

NOT SATISFACTORY!

Lag compensator can reduce steady-state error.



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How to design lag compensator

- Lag compensator $C_{Lag}(s) = \frac{s+z}{s+p}$
- We want to increase ramp-error constant

$$K_v = \lim_{s \rightarrow 0} sG(s)C_{Lead}(s)C_{Lag}(s) = 5.02 \cdot \frac{z}{p} > 50$$

Take, for example, $z=10p$.

- We do not want to change CL pole location s_1 so much (already satisfactory transient).

$$\left. \begin{aligned} 1 + G(s_1)C_{Lead}(s_1) &= 0 \\ C_{Lag}(s_1) &\approx 1 \end{aligned} \right\} \rightarrow 1 + G(s_1)C_{Lead}(s_1)C_{Lag}(s_1) \approx 0$$

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Guidelines to choose z and p

- The zero and the pole of a lag compensator should be **close to each other**, for

$$C_{Lag}(s_1) \approx 1$$
- The pole of a lag compensator should be **close to the origin**, to have a large ratio z/p, leading to a large ramp-error constant K_v .
- However, the pole of a lag compensator too close to the origin may be problematic:
 - Difficult to realize (recall op-amp realization)
 - Slow settling (due to closed-loop pole near the origin)

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Root locus with lag compensator

- Without compensator
 - With compensator
-
- $-\theta_1 - \theta_2 - \theta_3 = 180$
 $-\theta_1 - \theta_2 - \theta_3 + \theta_z - \theta_p \approx 180$

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How to design lag compensator

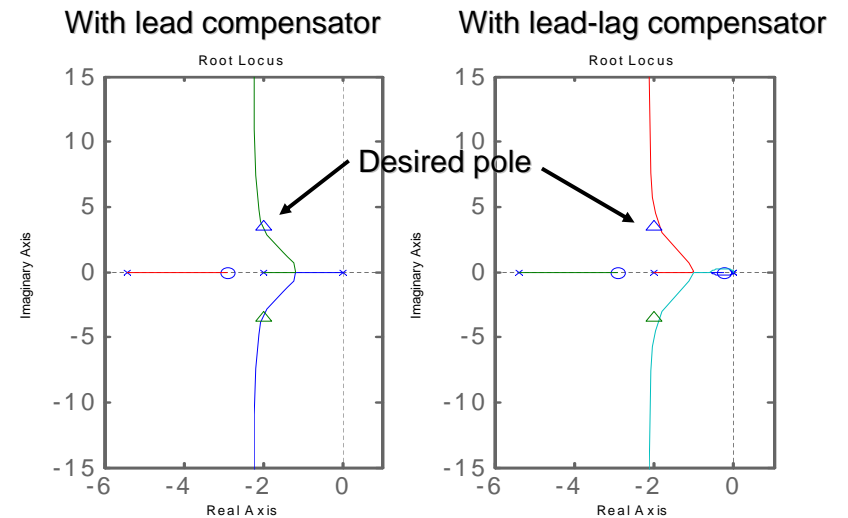
- For the desired CL pole $s_1 = -2 + 2\sqrt{3}j$
- $$C_{Lag}(s_1) \approx 1 \iff \left| \frac{s_1 + 10p}{s_1 + p} \right| \approx 1 \quad \angle \left(\frac{s_1 + 10p}{s_1 + p} \right) \approx 0$$
- Take a small p (by trial-and-error!)

$$p = 0.025 \implies \left| \frac{s_1 + 10p}{s_1 + p} \right| = 0.97 \quad \angle \left(\frac{s_1 + 10p}{s_1 + p} \right) \approx -2.88^\circ$$
 - Lead-lag controller

$$C_{LL}(s) = 4.675 \frac{s + 2.9}{s + 5.4} \cdot \frac{s + 0.25}{s + 0.025}$$

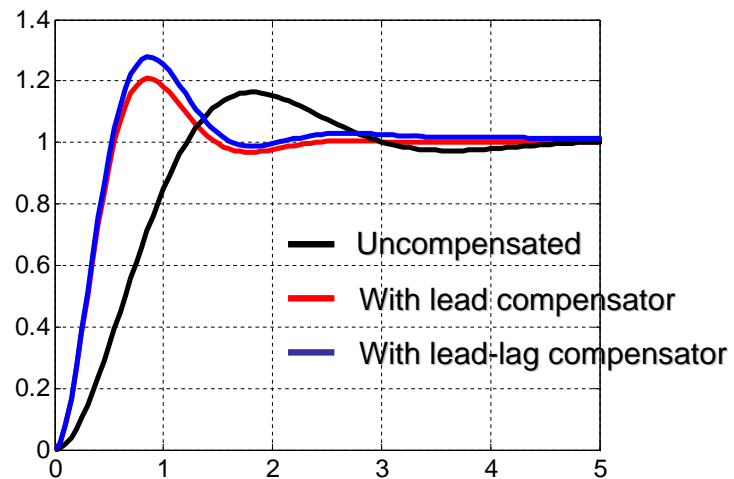
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Root locus



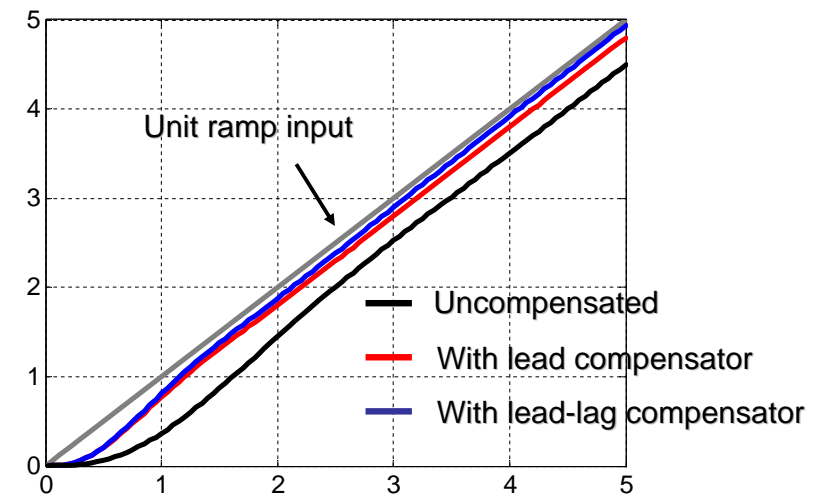
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Comparison of step responses



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Comparison of ramp responses



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Summary and exercises

- Controller design based on root locus
 - Lag compensator design
 - **Lag compensator improves steady state error.**
 - Lead-lag compensator design
 - **Lead-lag compensator improves stability, transient and steady-state responses.**
- Next, frequency response and Bode plot

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